

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	10/776,572
Filing Date	02-11-2004
First Named Inventor	Jaiprakash et al.
Art Unit	2815
Examiner Name	TBA
Attorney Docket Number	112020.144US2 NAN-20

	US-6,559,468 B1	05-06-2003	KUEKES et al.	
	US-6,750,471B2	06-15-2004	BETHUNE et al.	
	US-6,159,620	12-12-2000	HEATH et al.	
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	US-6,232,706	05-15-2001	DAI et al.	
	US-6,183,714	02-06-2000	SMALLEY et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ^{2(f known)}			
		WO 01/44796 A1	06-21-2001	Board of Trustees of the Leland Stanford Junior University	
		WO 01/03208 A1	01-11-2001	President and Fellows of Harvard	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	A1	CHOI, W.B. et al., "Carbon-nanotube-based nonvolatile memory with oxide-nitride-film and nanoscale channel," <i>Appl. Phys. Lett.</i> , 2003, Vol. 82(2), pp.275-277.	
	A2	DEQUESNES, M. et al., "Calculation of pull-in voltages for carbon-nanotube-based nanoelectromechanical switches," <i>Nanotechnology</i> , 2002, Vol. 13, pp. 120-131.	
	A3	DEQUESNES, M. et al., "Simulation of carbon nanotube-based nanoelectromechanical switches," <i>Computational Nanoscience and Nanotechnology</i> , 2002, pp. 383-386.	
	A4	WOLF, S., Silicon Processing for the VLSI Era; Volume 2 - Process Integration, Multi-Level-Interconnect Technology for VLSI and ULSI, 1990, Section 4.3 Materials for Multilevel Interconnect Technologies, pp. 189-191, Lattice Press, Sunset Beach	
	A5	WOLF, S., Silicon Processing for the VLSI Era; Volume 2 - Process Integration, 1990, Section 4.7 Manufacturing Yield and Reliability Issues of VLSI Interconnects, pp. 260-273, Lattice Press, Sunset Beach	

Examiner Signature		Date Considered	2/2/2005
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	A6	ROBINSON, L.A.W., "Self-Aligned Electrodes for Suspended Carbon Nanotube Structures," <i>Microelectronic Engineering</i> , 2003, Vols. 67-68, pp. 615-622.	
	A7	CUI, J.B. et al., "Carbon Nanotube Memory Devices of High Charge Storage Stability," <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(17), pp. 3260-3262.	
	A8	TOUR, J. M. et al., "NanoCell Electronic Memories," <i>J. Am. Chem. Soc.</i> , 2003, Vol. 125, pp. 13279-13283.	
	A9	RUECKES, T., et al., "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing" <i>Science</i> , 2000, Vol. 289, pp. 94-97.	
	A10	FAN, S. et al., "Carbon nanotube arrays on silicon substrates and their possible application," <i>Physica E</i> , 2000, Vol. 8, pp. 179-183.	
	A11	ZHAN, W. et al., "Microelectrochemical Logic Circuits," <i>J. Am. Chem. Soc.</i> , 2003, Vol. 125, pp. 9934-9935.	
	A12	SOH, H. T. et al., "Integrated nanotube circuits: Controlled growth and ohmic contacting of single-walled carbon nanotubes," <i>Appl. Phys. Lett.</i> , 1999, Vol. 75(5), pp. 627-629.	
	A13	KINARET, J.M. et al., "A carbon-nanotube-based nanorelay", <i>Appl. Phys. Lett.</i> , 2003, Vol. 82(8), pp. 1287-1289.	
	A14	FRANKLIN, N. R. et al., "Integration of suspended carbon nanotube arrays into electronic devices and electromechanical systems," <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(5), pp. 913-915.	
	A15	AVOURIS, Ph., "Carbon nanotube electronics," <i>Chem. Physics</i> , 2002, Vol. 281, pp. 429-445.	
	A16	DAI, H. et al., "Controlled Chemical Routes to Nanotube Architectures, Physics, and Devices," <i>J. Phys. Chem. B</i> , 1999, Vol. 103, pp. 111246-11255.	
	A17	HOMMA, Y. et al., "Growth of Suspended Carbon Nanotubes Networks on 100-nm-scale Silicon Pillars," <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(12), pp. 2261-2263.	
	A18	AJAYAN, P.M., et al., "Nanometre-size tubes of carbon," <i>Rep. Prog. Phys.</i> , 1997, Vol. 60, pp. 1025-1062.	
	A19	SREEKUMAR, T.V., et al., "Single-wall Carbon Nanotube Films", <i>Chem. Mater.</i> 2003, Vol. 15, pp. 175-178.	
	A20	VERISSIMO-ALVES, M. et al., "Electromechanical effects in carbon nanotubes: <i>Ab initio</i> and analytical tight-binding calculations," <i>Phys. Rev. B</i> , 2003, Vol. 67, pp. 161401-1 - 161401-4.	
	A21	FUHRER, M.S. et al., "High-Mobility Nanotube Transistor Memory," <i>Nano Letters</i> , 2002, Vol. 2(7), pp. 755-759.	

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	A22	RADOSAVLJEVIC, M. et al., "Nonvolatile molecular memory elements based on ambipolar nanotube field effect transistors," <i>Nano Letters</i> , 2002, Vol. 2(7), pp. 761-764.	
	A23	FARAJIAN, A. A. et al., "Electronic transport through bent carbon nanotubes: Nanoelectromechanical sensors and switches," <i>Phys. Rev. B</i> , 2003, Vol. 67, pp. 205423-1 - 205423-6.	
	A24	FISCHER, J.E. et al., "Magnetically aligned single wall carbon nanotube films: Preferred orientation and anisotropic transport properties," <i>Journal of Appl. Phys.</i> , 2003, Vol. 93(4), pp. 2157-2163.	
	A25	LEE, K.H. et al., "Control of growth orientation for carbon nanotubes," <i>Appl. Phys. Lett.</i> , 2003, Vol. 82(3), pp. 448-450.	
	A26	CASAVANT, M.J. et al., "Neat macroscopic membranes of aligned carbon nanotubes," <i>Journal of Appl. Phys.</i> , 2003, Vol. 93(4), pp. 2153-2156.	
	A27	CHEN, R. J. et al., "Noncovalent Sidewall Functionalization of Single-Walled Carbon Nanotubes for Protein Immobilization," <i>J. Am. Chem. Soc.</i> , 2001, Vol. 123, pp. 3838-3839.	
	A28	Zhang, Y. and Hongjie Dai. "Formation of metal nanowires on suspended single-walled carbon nanotubes." <i>Applied Physics Letters</i> (6 Nov. 2000): 3015 - 3017.	

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